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6. (Amended) A bus master control device for controlling an operation of a bus master for transferring data through a bus, the device comprising:

bus occupation request means for outputting a signal requesting to occupy the bus in response to a data transfer request;

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data transfer means for transferring a first predetermined number of data items of all data items to be transferred while the bus master is occupying the bus without interruption based on a predetermined period of time during which said data transfer means is allowed to continuously occupy the bus; [and]

first determination means for determining if the first predetermined number of data items have been transferred; and

bus release instruction means for outputting a signal instructing to release the bus after it is determined that the first predetermined number of data items have been transferred.

9. (Amended) A bus master control device according to claim 6, wherein:

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the data transfer means [comprising:] comprises a first counter for counting a number of data items which have been transferred out of the first predetermined number of data items[;], and

the first determination means [for determining] determines if the first predetermined number of data items have been transferred based on an output from the first counter.

REMARKS

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Claims 1-10 are presently pending in this utility patent application. By way of this response, the title of the invention has been amended to provide a clear indication of the invention to which the claims are directed and Claims 1, 6 and 9 have been revised. After entry of the amendments to Claims 1, 6 and 9, claims 1-10 (2 independent claims; 10 total claims) remain in the application.

Reconsideration is respectfully requested in light of the foregoing amendments and the following remarks. The foregoing amendments and following remarks are believed to be fully responsive to the outstanding Office Action mailed on September 4, 1998.

I. NEW TITLE OF THE INVENTION REQUIREMENT

The Examiner required a new title of the invention as the originally filed title of the invention was believed to be non-descriptive. In view of this requirement, the title has been amended to reflect the title as suggested by the Examiner.

II. REJECTIONS UNDER 35 U.S.C. 103(a)

The Examiner rejected claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al., U.S. Patent No. 5,287,486, issued February 15, 1994 (hereinafter "the Yamasaki reference"), in view of Delp et al., U.S. Patent No. 5,752,078, issued May 12, 1998 (hereinafter "the Delp reference"). These rejections are respectfully traversed.

The Examiner primarily cites the Yamasaki reference as teaching the invention as claimed and introduces the Delp reference for the limited purpose of teaching a partial direct memory access (DMA) transfer which is acknowledged by the Examiner to be absent from the teachings of the Yamasaki reference. It is the Examiner's contention that the Yamasaki reference teaches the invention as claimed, including a method of transferring data through a bus as recited in independent Claim 1 and a bus master control device for controlling an operation of a bus master for transferring data through a bus as recited in independent Claim 6. However, the Yamasaki reference merely provides for a direct memory access controller that is operable in a burst mode in which the central processing unit is cut off from the buses while one of the input/output (I/O) devices is connected to the buses for a predetermined period. (Yamasaki, Column 2, lines 40-45). More specifically, the

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Yamasaki reference provides that in response to a DMA request from one of the I/O devices, the memory and the I/O device are connected via buses to perform data transfer in the burst mode and when a time up signal is outputted from the programmed timer circuit or external program during the burst mode, the CPU is connected to the buses while the I/O device is cut off from the buses. (Yamasaki, Column 2, lines 55-62).

In contrast to the method and device of the Yamasaki reference and the Delp reference, the Applicants' invention of amended Claims 1 and 6 operates such that a first device that is currently occupying the bus is not forced to release the bus to a second device based on a predetermined period of time during which the first device is allowed to continuously occupy the bus. As explained in the Applicants' Specification, the number of data items to be successively transferred in a single subset transfer is ensured since completion of a data subset transfer is detected based on the number of data items transferred rather than a period of time. (Applicants' Specification, page 27, lines 18-22.) In this manner, data may be transferred more efficiently when each data transfer operation transfers a particular number of data items (e.g., 8 bytes) so as to better correspond to the data processing procedures of the CPU or the peripheral unit. (Applicants' Specification, page 27, lines 22-26.)

It is respectfully submitted that the Examiner's reliance on the Yamasaki reference Application, either singly or in combination with the Delp reference, does not establish a prima facie case of obviousness as this reference does not disclose, teach, or suggest transferring a first predetermined number of data items of all data items to be transferred "without interruption based on a predetermined period of time during which the first device is allowed to continuously occupy the bus" or "without interruption based on a predetermined period of time during which said data transfer means is allowed to continuously occupy the bus" as recited in amended Claims 1 and 6, respectively. In fact, the Yamasaki reference teaches away from transferring a predetermined

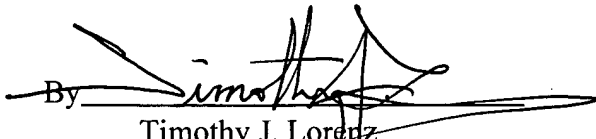


number of data items of all data items to be transferred without interruption based on a predetermined period of time. Specifically, the Yamasaki reference provides that "the central processing unit is cut off from the buses while one of the input/output devices is connected to the buses for a predetermined period of time." (Yamasaki, Column 2, lines 41-44, emphasis added.) Furthermore, the references lack any suggestion or motivation to modify the methods and apparatus presented in the Yamasaki reference or the Delp reference along the lines of the invention recited in Applicants' amended claims, and one skilled in the art would not have been independently motivated to make such modifications. Therefore, it is respectfully submitted that independent claims 1 and 6, and claims 2-5 and 7-10 depending therefrom, are allowable over the cited references, and the Examiner is requested to withdraw the § 103 rejections.

III. CONCLUSION

In view of the foregoing, it is respectfully requested that the present application is now in condition for allowance. Such allowance is therefore courteously solicited at this time. The Examiner is encouraged to call the undersigned if there are additional matters to be addressed in this application.

Respectfully submitted,

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